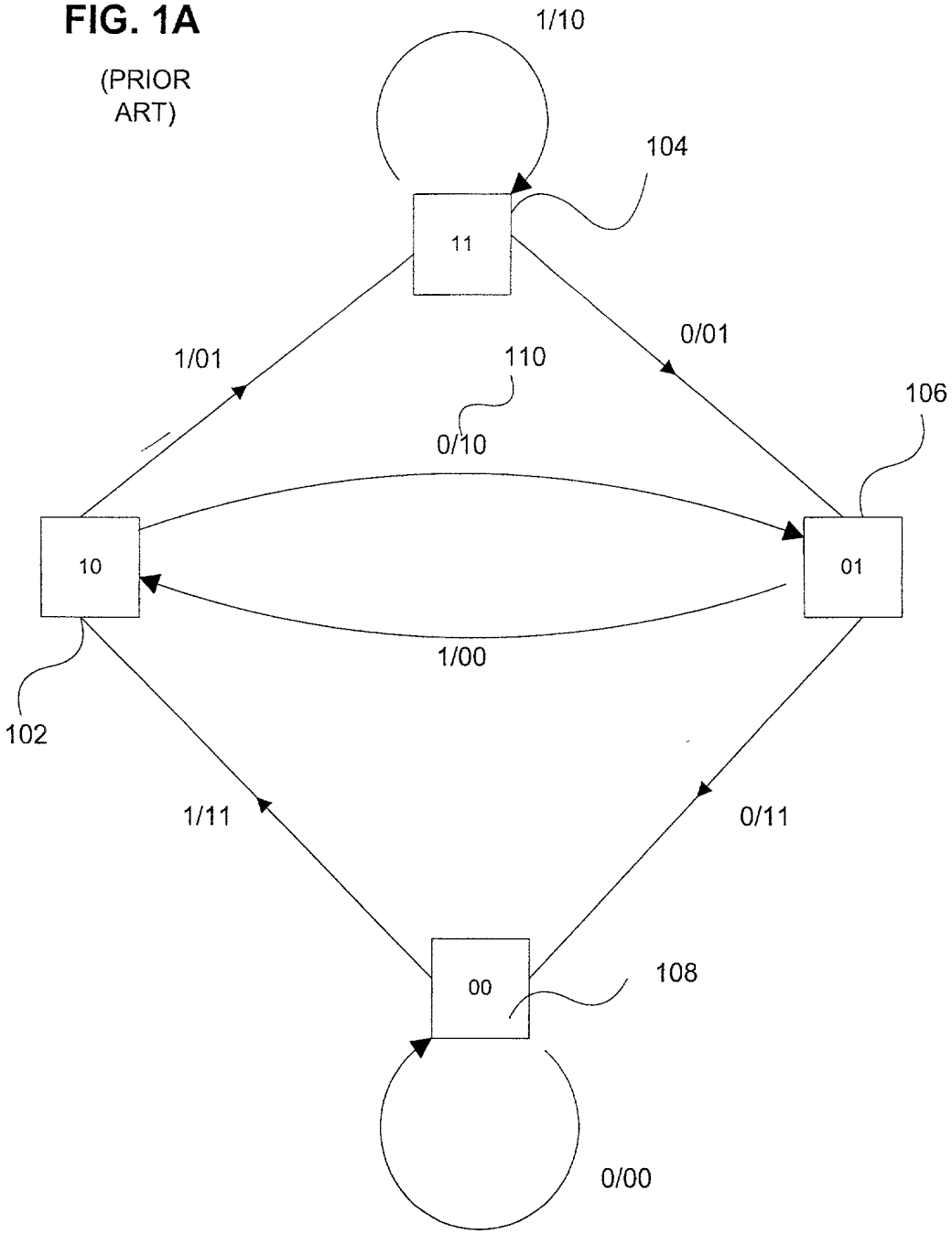
FIG. 1A

(PRIOR ART)



INPUT BIT	INITIAL STATE	NEXT STATE	OUTPUT CODEWORD
0	00	00	00
1	00	10	11
0	01	00	11
1	01	10	00
0	10	01	10
1	10	11	01
0	11	01	01
1	11	11	10

FIG. 1B (PRIOR ART)

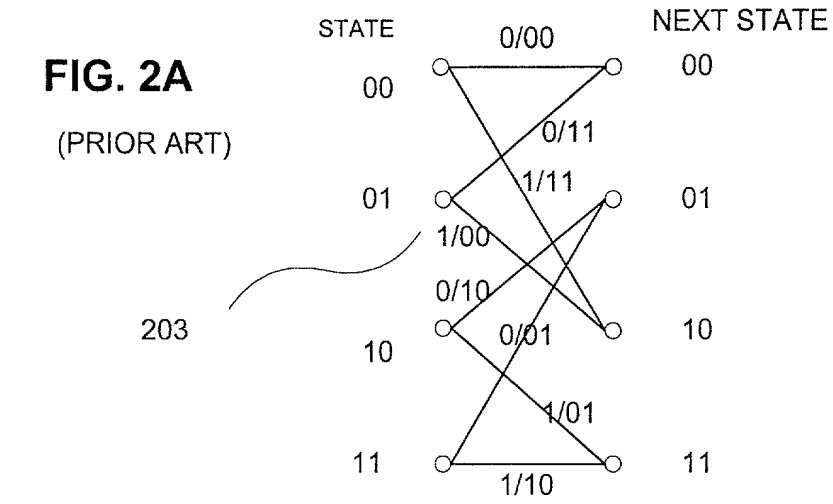


FIG. 2A

(PRIOR ART)

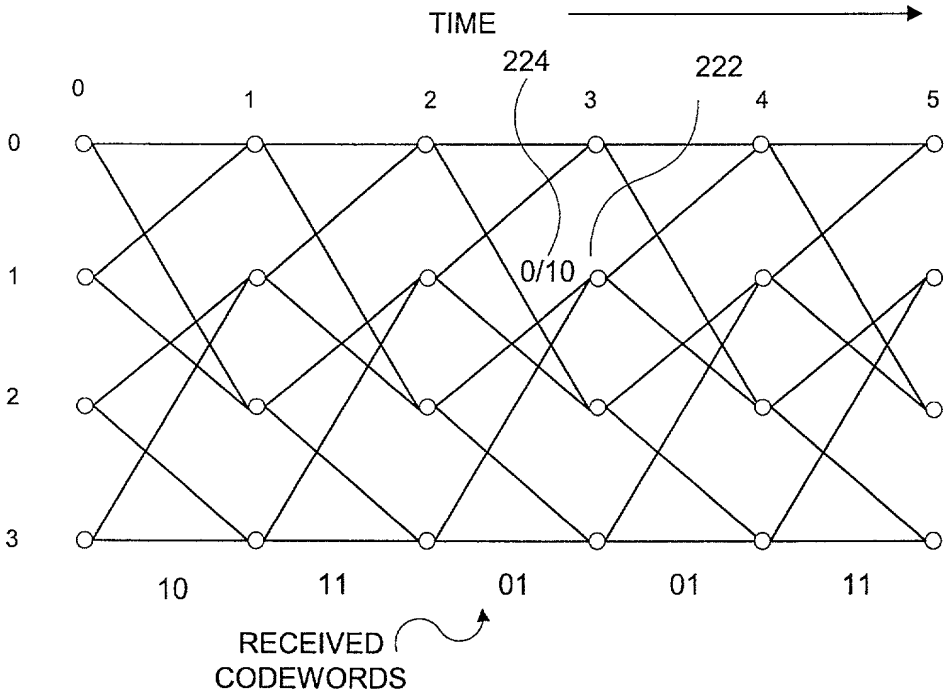


FIG. 2B (PRIOR ART)

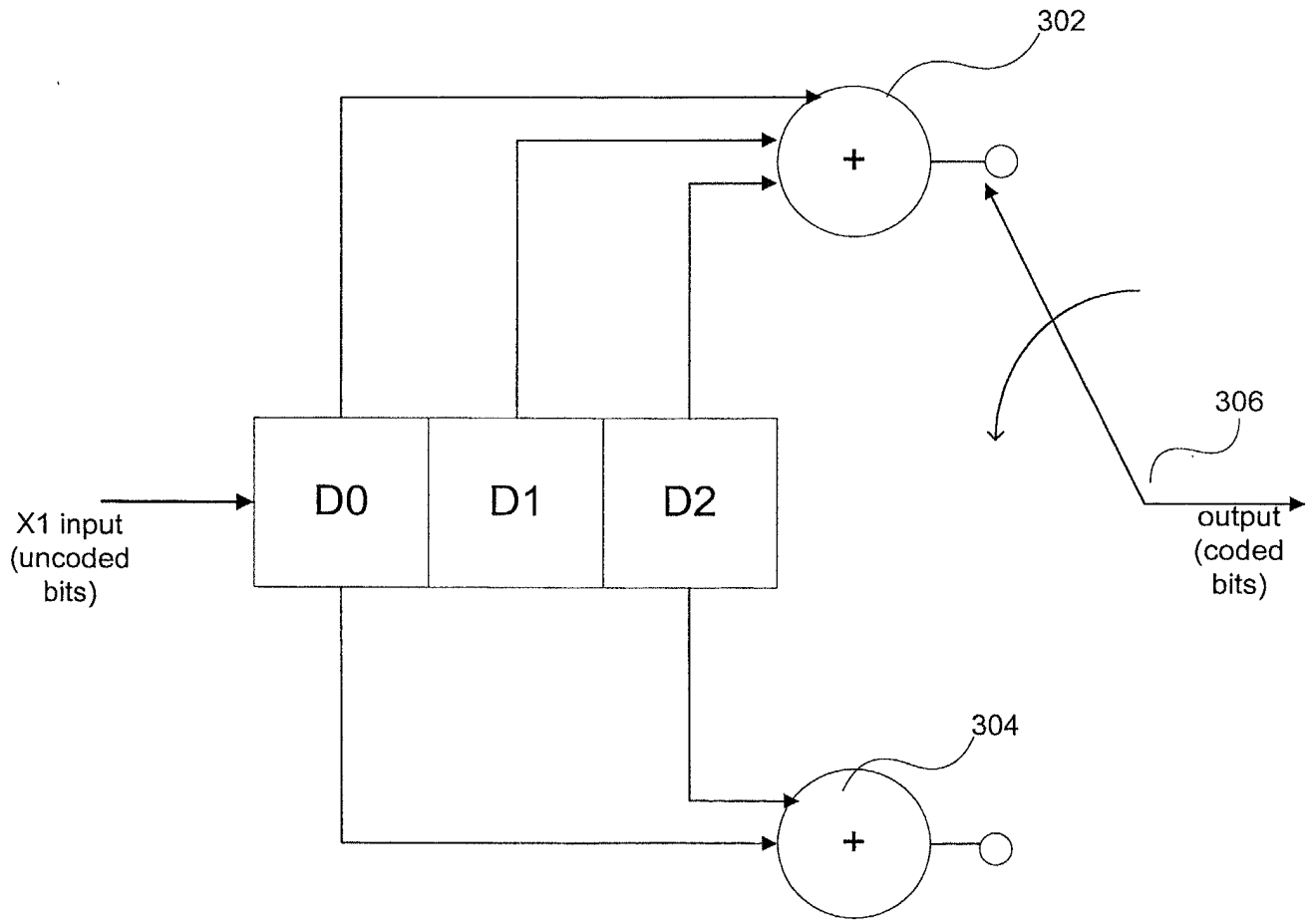


FIG. 3 (Prior Art)

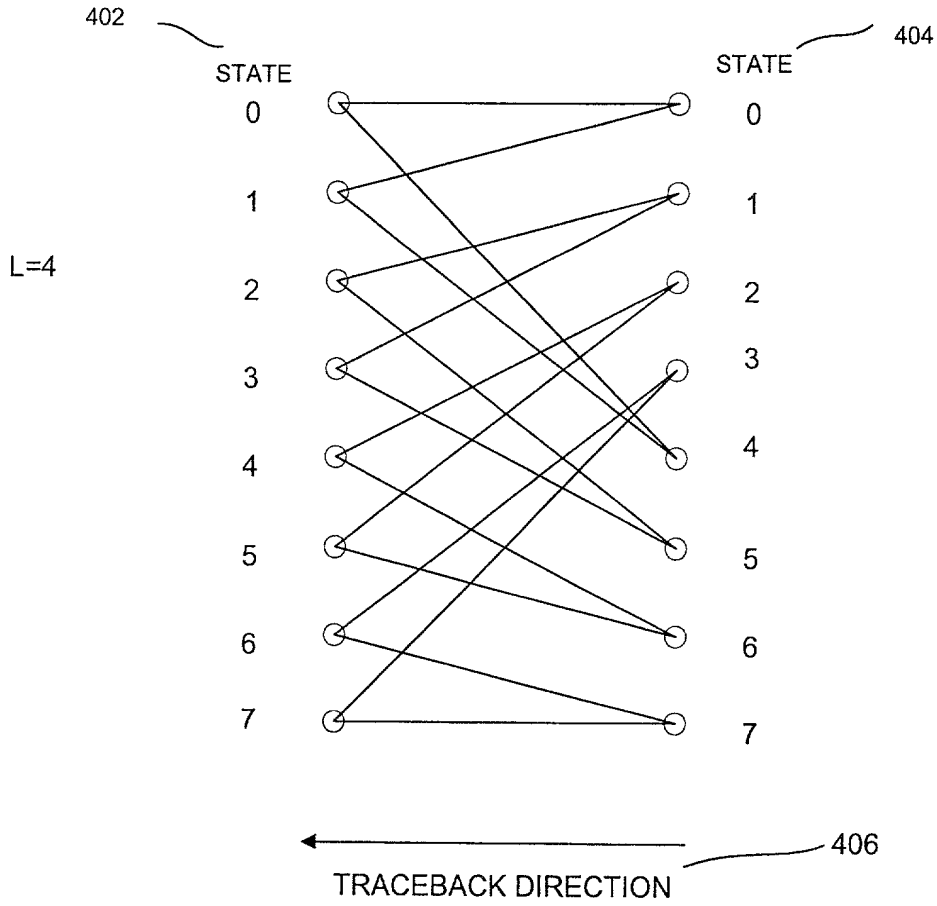

402
STATE
404
STATE
0
1
2
3
4
5
6
7
L=4
0
1
2
3
4
5
6
7
406
TRACEBACK DIRECTION

FIG. 4A

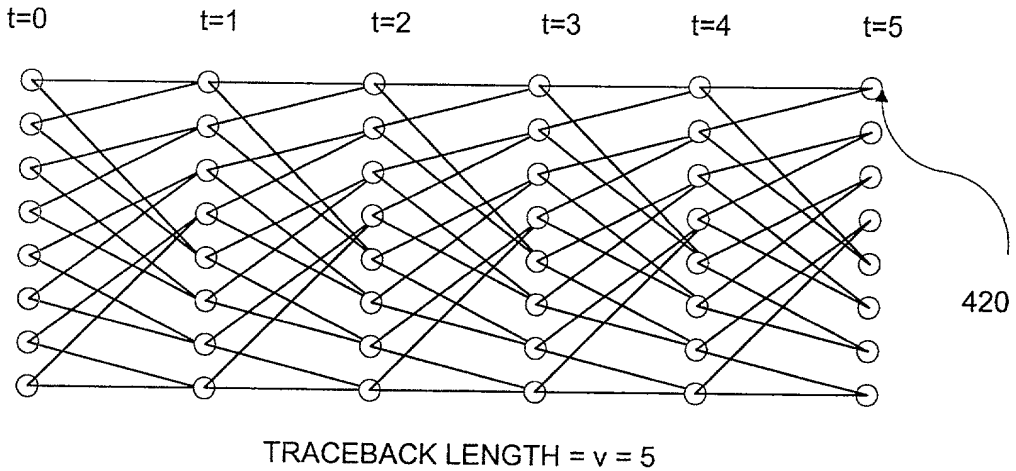

t=0
t=1
t=2
t=3
t=4
t=5
420
TRACEBACK LENGTH = v = 5

FIG. 4B

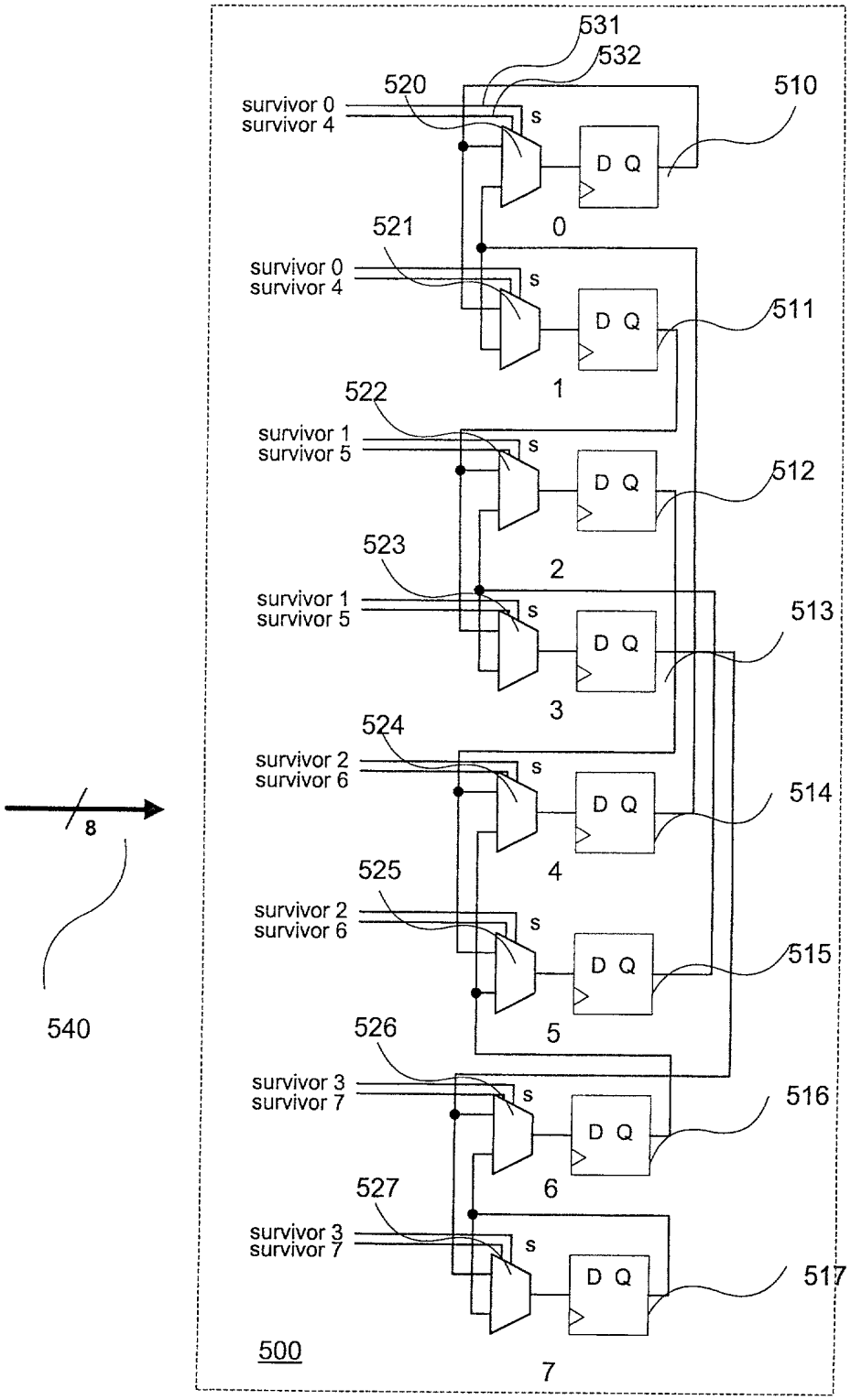

531
532
520
510
survivor 0
survivor 4
s
D Q
0
521
survivor 0
survivor 4
511
1
522
survivor 1
survivor 5
512
2
523
survivor 1
survivor 5
513
3
524
survivor 2
survivor 6
514
4
525
survivor 2
survivor 6
515
5
526
survivor 3
survivor 7
516
6
527
survivor 3
survivor 7
517
7
500
8
540

FIG. 5

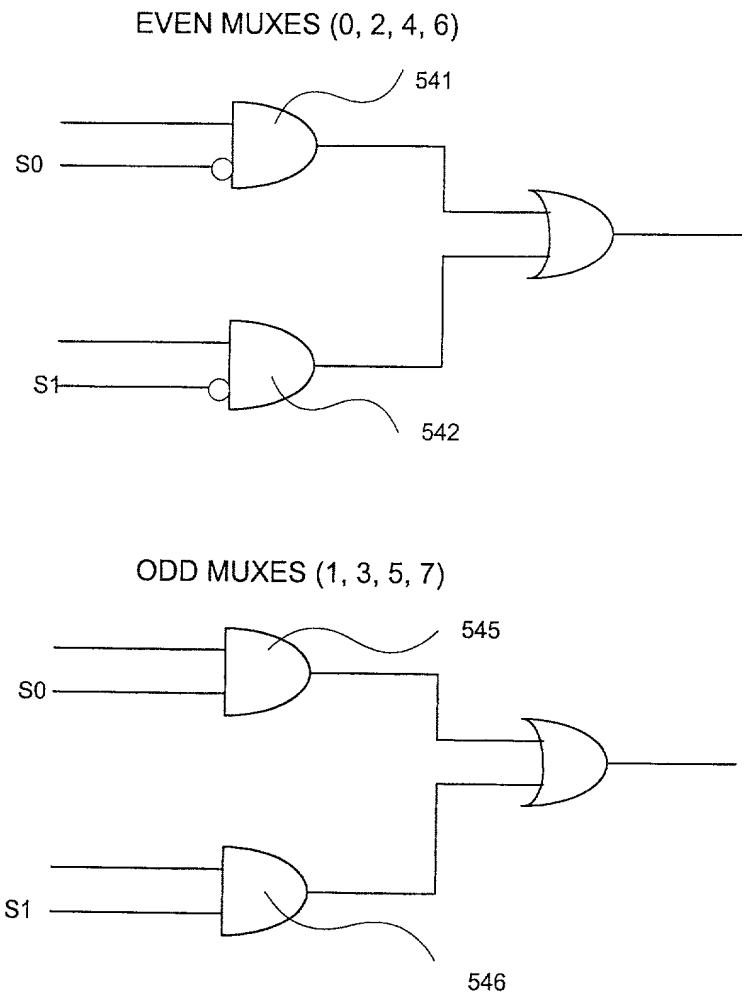


FIG. 5A

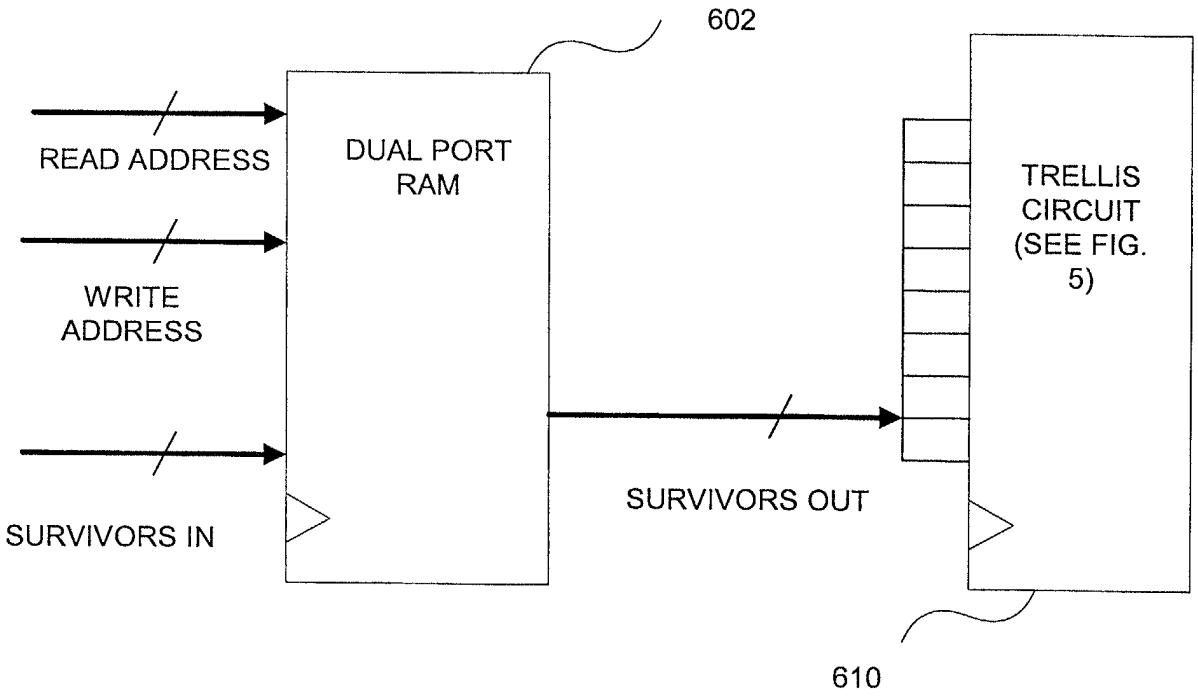


FIG. 6

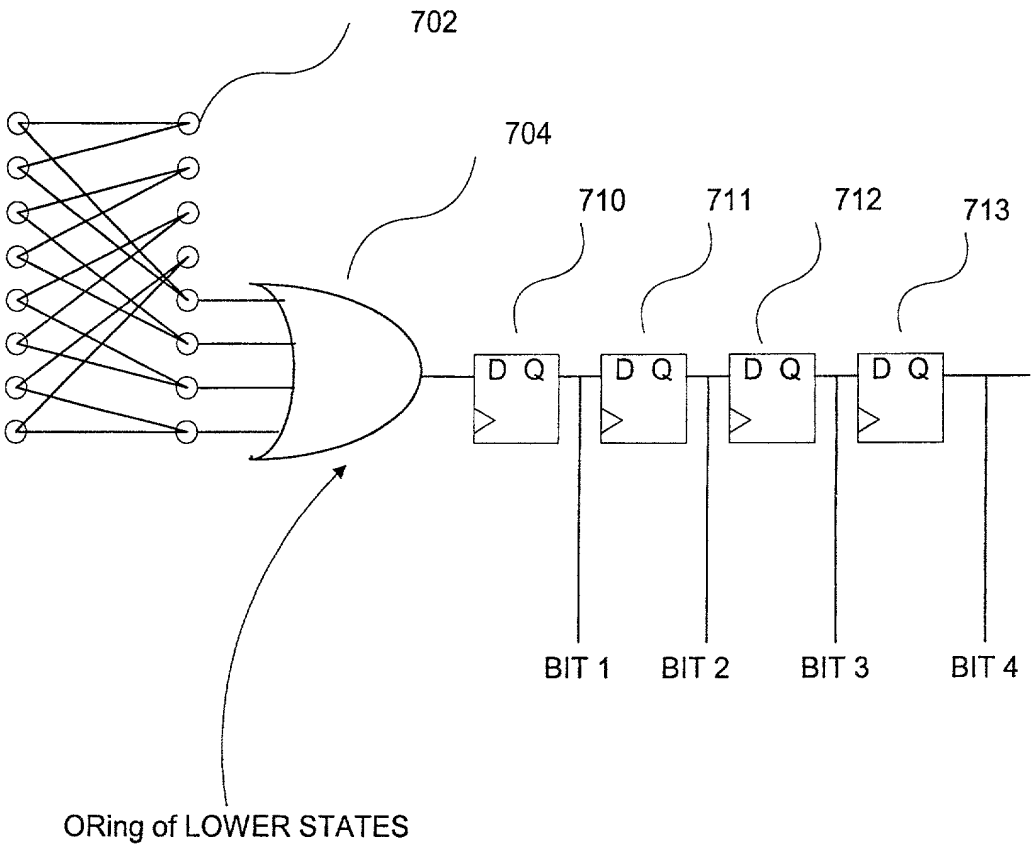

702
704
710
711
712
713
D Q
D Q
D Q
D Q
BIT 1
BIT 2
BIT 3
BIT 4
ORing of LOWER STATES

FIG. 7

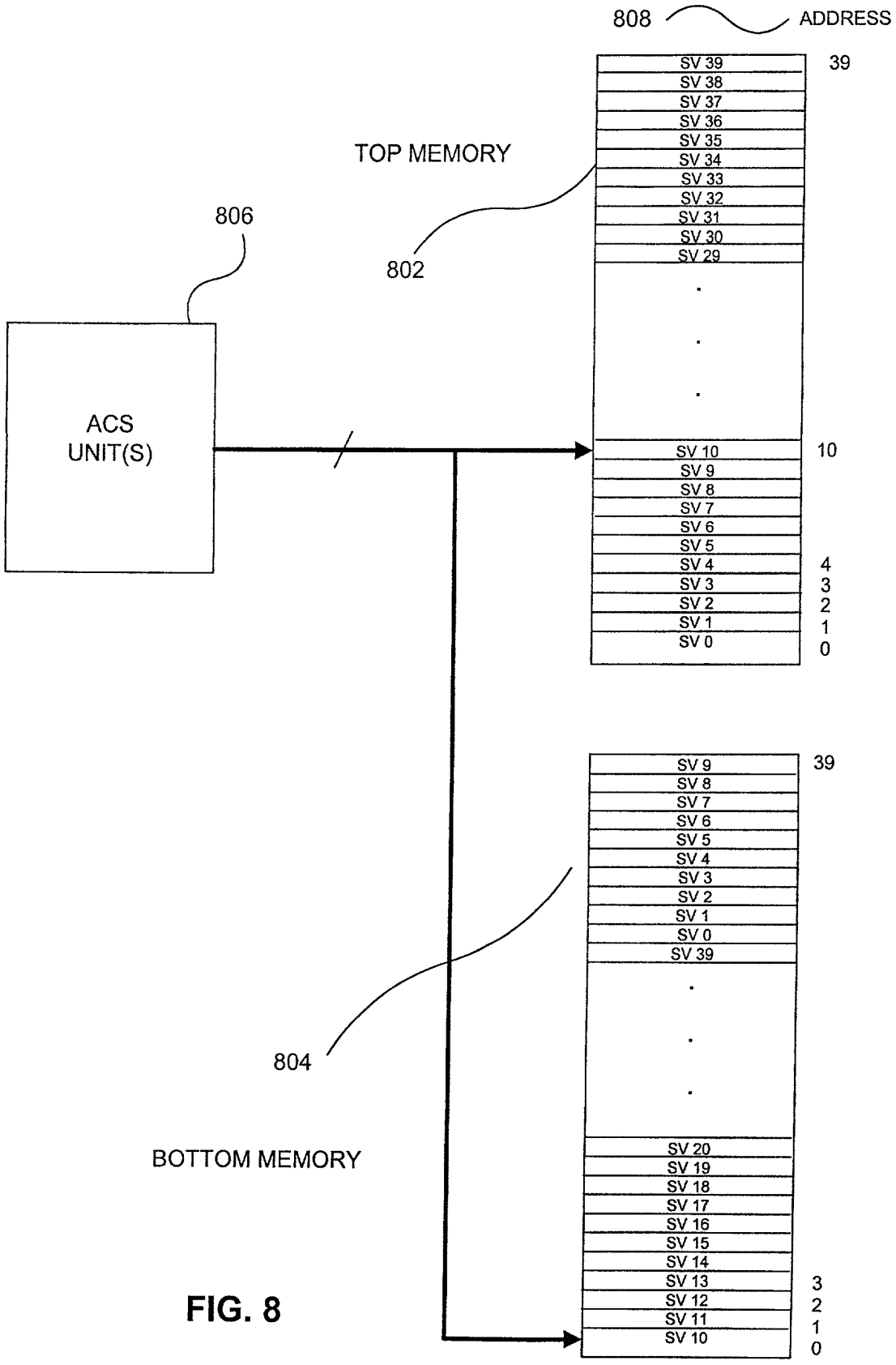

808
ADDRESS
SV 39
SV 38
SV 37
SV 36
SV 35
SV 34
SV 33
SV 32
SV 31
SV 30
SV 29
39
TOP MEMORY
806
802
ACS
UNIT(S)
SV 10
SV 9
SV 8
SV 7
SV 6
SV 5
SV 4
SV 3
SV 2
SV 1
SV 0
10
4
3
2
1
0
SV 9
SV 8
SV 7
SV 6
SV 5
SV 4
SV 3
SV 2
SV 1
SV 0
SV 39
39
804
BOTTOM MEMORY
SV 20
SV 19
SV 18
SV 17
SV 16
SV 15
SV 14
SV 13
SV 12
SV 11
SV 10
3
2
1
0

FIG. 8

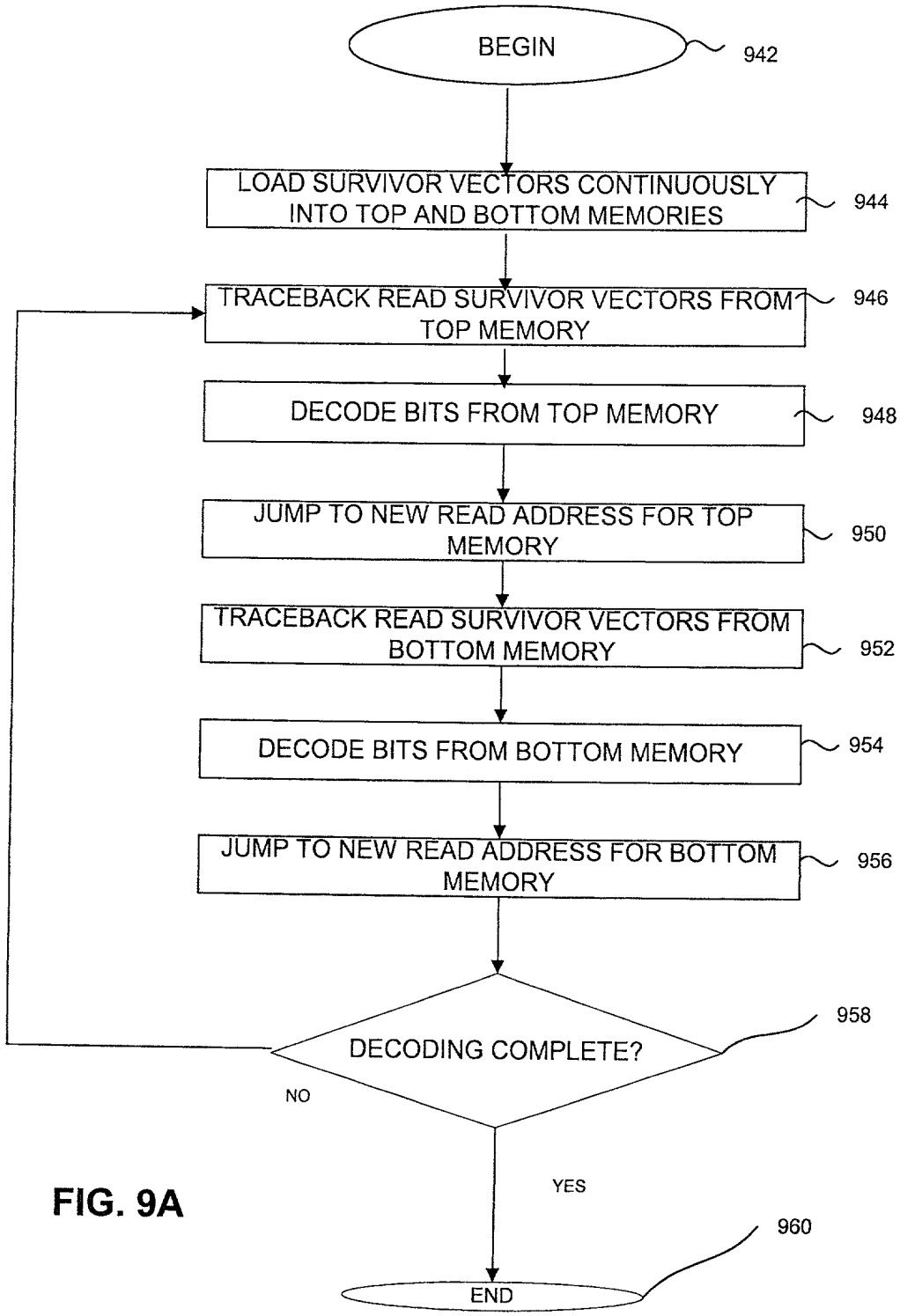

BEGIN
942
LOAD SURVIVOR VECTORS CONTINUOUSLY INTO TOP AND BOTTOM MEMORIES
944
TRACEBACK READ SURVIVOR VECTORS FROM TOP MEMORY
946
DECODE BITS FROM TOP MEMORY
948
JUMP TO NEW READ ADDRESS FOR TOP MEMORY
950
TRACEBACK READ SURVIVOR VECTORS FROM BOTTOM MEMORY
952
DECODE BITS FROM BOTTOM MEMORY
954
JUMP TO NEW READ ADDRESS FOR BOTTOM MEMORY
956
DECODING COMPLETE?
958
NO
YES
END
960

FIG. 9A

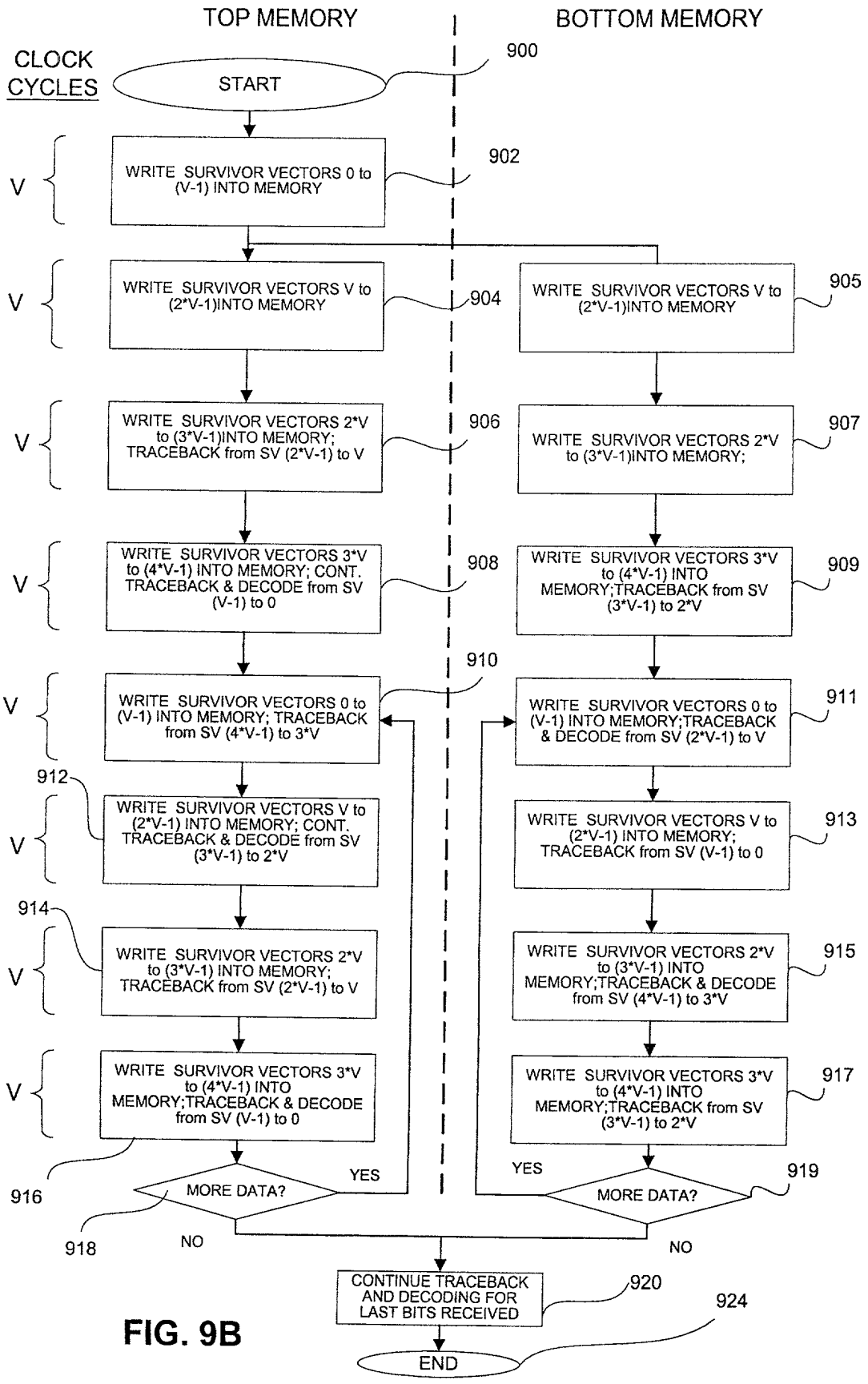

TOP MEMORY
BOTTOM MEMORY
CLOCK CYCLES
START
900
WRITE SURVIVOR VECTORS 0 to (V-1) INTO MEMORY
902
V
WRITE SURVIVOR VECTORS V to (2*V-1)INTO MEMORY
904
WRITE SURVIVOR VECTORS V to (2*V-1)INTO MEMORY
905
WRITE SURVIVOR VECTORS 2*V to (3*V-1)INTO MEMORY; TRACEBACK from SV (2*V-1) to V
906
WRITE SURVIVOR VECTORS 2*V to (3*V-1)INTO MEMORY;
907
WRITE SURVIVOR VECTORS 3*V to (4*V-1) INTO MEMORY; CONT. TRACEBACK & DECODE from SV (V-1) to 0
908
WRITE SURVIVOR VECTORS 3*V to (4*V-1) INTO MEMORY;TRACEBACK from SV (3*V-1) to 2*V
909
910
WRITE SURVIVOR VECTORS 0 to (V-1) INTO MEMORY; TRACEBACK from SV (4*V-1) to 3*V
WRITE SURVIVOR VECTORS 0 to (V-1) INTO MEMORY;TRACEBACK & DECODE from SV (2*V-1) to V
911
912
WRITE SURVIVOR VECTORS V to (2*V-1) INTO MEMORY; CONT. TRACEBACK & DECODE from SV (3*V-1) to 2*V
WRITE SURVIVOR VECTORS V to (2*V-1) INTO MEMORY; TRACEBACK from SV (V-1) to 0
913
914
WRITE SURVIVOR VECTORS 2*V to (3*V-1) INTO MEMORY; TRACEBACK from SV (2*V-1) to V
WRITE SURVIVOR VECTORS 2*V to (3*V-1) INTO MEMORY;TRACEBACK & DECODE from SV (4*V-1) to 3*V
915
WRITE SURVIVOR VECTORS 3*V to (4*V-1) INTO MEMORY;TRACEBACK & DECODE from SV (V-1) to 0
WRITE SURVIVOR VECTORS 3*V to (4*V-1) INTO MEMORY;TRACEBACK from SV (3*V-1) to 2*V
917
916
MORE DATA?
YES
NO
918
YES
MORE DATA?
919
NO
CONTINUE TRACEBACK AND DECODING FOR LAST BITS RECEIVED
920
924
END

FIG. 9B

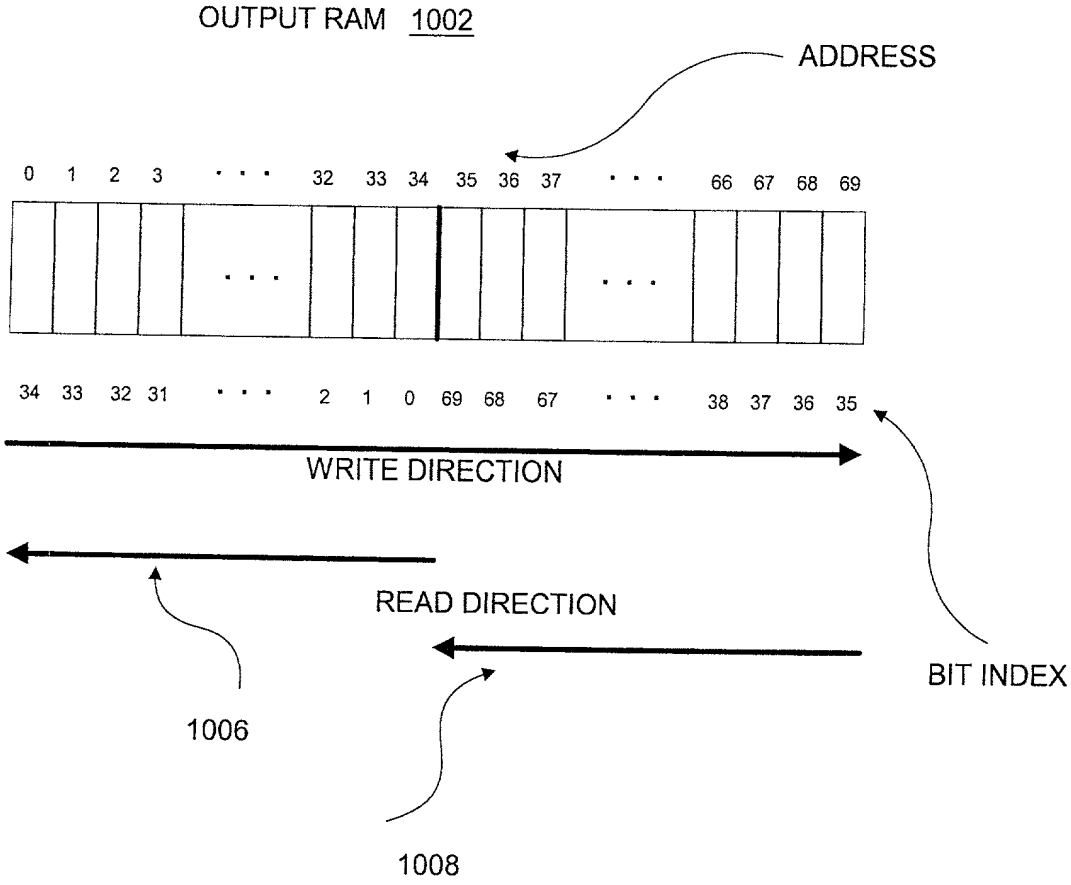

OUTPUT RAM 1002
ADDRESS
0 1 2 3 . . . 32 33 34 35 36 37 . . . 66 67 68 69
34 33 32 31 . . . 2 1 0 69 68 67 . . . 38 37 36 35
WRITE DIRECTION
READ DIRECTION
BIT INDEX
1006
1008

FIG. 10